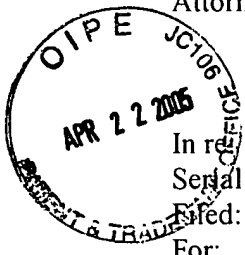


C985
JRW

Attorney's Docket No. 5347-210

PATENT



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re: Blanton
Serial No.: 09/866,357
Filed: May 25, 2001

U.S. Patent No.: 6,836,856
Issued: December 28, 2004

For: *Methods for Characterizing, Generating Test Sequences for, and/or
Simulating Integrated Circuit Faults Using Fault Tuples and
Related Systems and Computer Program Products*

Date: April 20, 2005

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

**ERRORS APPEARING IN PRINTED PAGES
OF THE LETTERS PATENT**

Sir:

It is noted that certain errors appear in the Letters Patent identified above as follows:

In the Claims:

Column 14, line 18 should read -- observable at a primary output, generating a --

Column 20, line 27 should read --comprises a portion of a path between at least one of the --

The above errors are mistakes on the part of the Patent Office but do not appear to merit a Certificate of Correction. It is respectfully requested, however, that this letter be placed on record in the file of this patent so that no question may arise as to the true meaning of the particular terms mentioned above as they appear in the patent.

Respectfully submitted,

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I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on April 20, 2005.

Joyce Pauli